# Shafiur Rahman

*Curriculum Vitae*

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## Education

2016–2021 **Ph.D. in Computer Science**, *University of California, Riverside*, CA, USA.
*Co-advisors: Dr. Nael Abu-Ghazaleh & Dr. Rajiv Gupta*

2016–2020 **M.S. in Computer Science**, *University of California, Riverside*, CA, USA.
*GPA: 3.95*

2009–2014 **B.S. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering and Technology*, Dhaka, Bangladesh.

## Research Interests

- Computer Architecture
- Hardware Accelerators
- Parallel and Distributed Systems
- Machine Learning and Artificial Intelligence

## Experiences

2021–Present **Research Scientist**, *Facebook*, Menlo Park, CA.
- Working in the System Infrastructure organization.

Summer, 2021 **Intern - Software Development Engineer**, *Micron Technology*, Allen, TX.
- Interned in the Advanced Computing and Emerging Memory Systems group.
- Worked with architectural simulators to aid in development and profiling of co-processor architecture.

Summer, 2020 **RAMP Next Generation Platforms Technology Intern**, *Western Digital*, Milpitas, CA.
- Interned in the Platforms and Systems Concepts Group.
- Developed RTL components for a prototype Fast-CNN accelerator.
- Analyzed popular convolutional neural network structures to identify common architectural modules.

2016–2021 **Graduate Student Researcher**, *University of California, Riverside*.
- Specialized in Computer Architecture, Hardware Accelerators, and Heterogeneous Systems.

2014–2015 **Software Engineer**, *Therap Services, LLC*, Dhaka, Bangladesh.
- Developed test automation frameworks using Selenium Webdriver and Ruby.
- Maintained stress-testing and load-management routine for web service.

## Publications

MICRO'21 **JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator**.
**Shafiur Rahman**, Mahbod Afarin, Nael Abu-Ghazaleh, Rajiv Gupta.
The 54th IEEE/ACM International Symposium on Microarchitecture (MICRO'21), October 2021.

MICRO'20 **GraphPulse: An Event-Driven Hardware Accelerator for Asynchronous Graph Processing**.
**Shafiur Rahman**, Nael Abu-Ghazaleh, Rajiv Gupta.
The 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO'20), October 2020.

MICRO'20 **BOW: Breathing Operand Windows to Exploit Bypassing in GPUs**.
Hodjat Asghari Esfeden, Amirali Abdolrashidi, **Shafiur Rahman**, Daniel Wong, Nael Abu-Ghazaleh
The 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO'20), October 2020.

TOMACS'19 **PDES-A: Accelerators for Parallel Discrete Event Simulation Implemented on FPGAs**.
**Shafiur Rahman**, Nael Abu-Ghazaleh, Walid Najjar.
ACM Transactions on Modeling and Computer Simulation (TOMACS), Volume 29, No. 2, April 2019.

PADS'17 **PDES-A: A Parallel Discrete Event Simulation Accelerator for FPGAs**.
**Shafiur Rahman**, Nael Abu-Ghazaleh, Walid Najjar.
2017 ACM SIGSIM Conference on Principles of Advanced Discrete Simulation, May 2017.

PRL'13 **A template matching approach of one-shot-learning gesture recognition**.
Upal Mahbub, Hafiz Imtiaz, Tonmoy Roy, **Md Shafiur Rahman**, Md. Atiqur Rahman Ahad.
Pattern Recognition Letters, Volume 34, Issue 15, November 2013.

ICIEV'13 **Temporal segmentation of gestures using gradient orientation of depth images** .
Tonmoy Roy, Upal Mahbub, **Md Shafiur Rahman**, Hafiz Imtiaz, Md. Atiqur Rahman Ahad.
2013 International Conference on Informatics, Electronics and Vision (ICIEV), May 2013.

ICIAE'13 **One-Shot-Learning Gesture Recognition Using Motion History Based Gesture Silhouettes** .
Upal Mahbub, Tonmoy Roy, **Md Shafiur Rahman**, Hafiz Imtiaz, Seiichi Serikawa, Md Atiqur Rahman Ahad.
The 1st International Conference on Industrial Application Engineering, March 2013.

SICE'12 **Gesture recognition with depth images — A simple approach**.
Upal Mahbub, Hafiz Imtiaz, Tonmoy Roy, **Md Shafiur Rahman**, Md Atiqur Rahman Ahad.
2012 SICE Annual Conference (SICE), August 2012.

## Honors and Awards

2016 **Dean's Distinguished Fellowship**, University of California, Riverside

2014 **Winner of Cadence Design Contest 2014 - Tensilica Design Project**
Cadence Design Systems India Ltd.
*For designing a non-linear Volterra adaptive filter using Tensilica Xtensa Dataplane Processor*

2013 **Dean's Award**, Department of Electrical and Electronics Engineering,
Bangladesh University of Engineering and Technology

## Professional Activities

**External Reviewer**

- Parallel Computing (Elsevier)
- IEEE International Parallel and Distributed Processing Symposium (IPDPS) 2021

## Skills and Abilities

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| Programming Languages | C, C++, Python, MATLAB, CUDA |
| Hardware Design | Verilog HDL, Chisel, Xilinx Vivado, Questa, Synopsis EDA Toolchain |
| Architectural Simulators | Structural Simulation Toolkit, Gem5 |