Shafiur Rahman

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Education

University of California, Riverside **Sep 2016 – Sep 2021**
PhD in Computer Science *Riverside, CA*
MS in Computer Science
Dissertation: *Hardware Acceleration of Irregular Applications Using Event-Driven Execution.*
Specialization: Computer Architecture, Hardware Accelerators, Parallel and Distributed Systems.

Bangladesh University of Engineering and Technology **Mar 2009 – Jun 2014**
BS in Electrical and Electronic Engineering *Dhaka, Bangladesh*

Professional Experiences

Meta **Oct 2021 – Nov 2022**
Research Scientist (Software Engineering), Video Infrastructure *Menlo Park, CA*

- Worked in the development and maintenance of a multi-tenant compute farm for video transcoding.
- Contributed to the design and implementation of the services and APIs for a large-scale distributed system with C++ and PHP as the primary coding language.
- Collaborated with cross-functional teams and internal clients for defining specifications and roadmaps.
- Carried out performance profiling and load testing for reliability analysis.

Micron Technology **Apr 2021 – Sep 2021**
Software Engineering Intern, Advanced Computing and Emerging Memory Systems. *Allen, TX*

- Helped building in-house simulators for x86 processor and near-memory computing architecture.
- Implemented cache coherence and data prefetching capabilities for the simulators.
- Benchmarked and analyzed x86 processor performance to validate simulator results.

Western Digital Research **Jun 2020 – Aug 2020**
Hardware Engineering Intern, Platforms and Systems Concepts. *Milpitas, CA*

- Designed modules from specification for a prototype Fast-CNN hardware accelerator.
- Performed RTL implementation, synthesis, and timing verification for modules.

Therap Services LLC **Jul 2014 – Dec 2015**
Software Engineer *Dhaka, Bangladesh*

- Developed test automation and load testing framework with Ruby and Selenium Webdriver.

Selected Research Projects

Event-Driven Graph Processing Framework

- Developed an event-driven processing model to support graph algorithms efficiently in hardware.
- Designed an accelerator architecture for scalable and optimized graph processing on FPGA and ASIC.
- Developed an MPI-driven cycle-accurate hardware simulator using Structural Simulation Toolkit (SST) framework for fast prototyping and scalability analysis of the architecture on large graphs.

Hardware Accelerator for Parallel Discrete Events Simulation

- Designed a generalized and modular accelerator architecture for Parallel Discrete Events Simulations.
- Built a framework using Verilog and Chisel for fast RTL development for reconfigurable platforms.
- Performed RTL Synthesis of the framework for FPGA and deployed on a *Convey Wolverine ® Coprocessor*.

One-shot Learning Gesture Recognition

- Extracted and characterized distinguishing features from motion-history-image of a gesture.
- Developed algorithms for real-time gesture recognition using one-shot learning techniques.

Selected Publications

- **CommonGraph: Graph Analytics on Evolving Data**
  Mahabod Afarin, Chao Gao, Shafiur Rahman, Nael Abu-Ghazaleh, Rajiv Gupta; 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems [**ASPLOS 2023**], March 2023. *(To appear)*
- **JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator**
  Shafiur Rahman, Mahabod Afarin, Nael Abu-Ghazaleh, Rajiv Gupta; International Symposium on Microarchitecture [**MICRO 2021**], October 2021.
- **GraphPulse: An Event-Driven Hardware Accelerator for Asynchronous Graph Processing**
  Shafiur Rahman, Nael Abu-Ghazaleh, Rajiv Gupta; International Symposium on Microarchitecture [**MICRO 2020**], October 2020.
- **BOW: Breathing Operand Windows to Exploit Bypassing in GPUs**
  Hodjat Asghari Esfeden, Amirali Abdolrashidi, Shafiur Rahman, Daniel Wong, Nael Abu-Ghazaleh; International Symposium on Microarchitecture [**MICRO 2020**], October 2020.
- **PDES-A: Accelerators for Parallel Discrete Event Simulation implemented on FPGAs**
  Shafiur Rahman, Nael Abu-Ghazaleh, Walid Najjar; ACM Transactions on Modeling and Computer Simulation [**TOMACS 2019**], Volume 29 Issue 2, April 2019.
- **PDES-A: a Parallel Discrete Event Simulation Accelerator for FPGAs**
  Shafiur Rahman, Nael Abu-Ghazaleh, Walid Najjar; ACM SIGSIM Conference on Principles of Advanced Discrete Simulation [**PADS 2017**], 2017. *[Best paper nominee]*
- **A Template Matching Approach of One-Shot-Learning Gesture Recognition**
  Upal Mahbub, Hafiz Imtiaz, Tonmoy Roy, Shafiur Rahman, Md Atiqur Rahman Ahad; Pattern Recognition Letters, Elsevier, Nov. 2013.

Technical Skills

- **Programming Languages:** C, C++, Python, MATLAB
- **Hardware Design & Verification:** Verilog HDL, Chisel, ModelSim, Xilinx Vivado
- **Simulation Frameworks:** Gem5, Structural Simulation Toolkit (SST), CACTI